D-A055 249 TRW INC LAWNDALE CALIF SEMICONDUCTOR DIV F/G 9/1
MONOLITHIC 20W 2GHZ TRANSISTOR AND MONOLITHIC 5W 4GHZ TRANSISTO--ETC(U)
JAN 78 G SCHREYER DAAB07-77-C-0431
UNCLASSIFIED NL

| OF |
AD
A055249

END
DATE
FILMED
7 -78
DDC

AD A055249

FOR FURTHER TRAN

AD A049630

AD A049630

(12)

(6) MONOLITHIC 20W 2GHz TRANSISTOR AND MONOLITHIC 5W 4GHz TRANSISTOR.

(9) QUARTERLY REPORT NO. 2
14 SEP[redacted] — 13 DEC[redacted]77,
CONTRACT No. DAAB07-77-C-0431

(15)

(10) George Schreyer

(11) Jan 78

(12) 20 p.

PREPARED FOR:

COMMUNICATIONS SYSTEMS PROCUREMENT BRANCH
PROCUREMENT AND PRODUCTION DIRECTORATE
US ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY 07703

DDC
JUN 16 1978
F

TRW SEMICONDUCTORS
DIVISION OF TRW INC.
14520 AVIATION BOULEVARD
LAWNDALE, CALIFORNIA 90260

APPROVED FOR PUBLIC RELEASE. DISTRIBUTION UNLIMITED.

AD No.
DDC FILE COPY

354 550

78 06 07 001

Disclaimer

The findings in this report are not to be construed as an official Department of the Army position, unless so designated by other authorized documents.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

Acknowledgement Statement

This project has been accomplished as part of the U.S. Army (Manufacturing and Technology) Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to insure the efficient production of current or future defense programs.

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER DAABO7-77-C-0431	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* MONOLITHIC 20W 2GHz TRANSISTOR and 5W 4GHz TRANSISTOR		5. TYPE OF REPORT & PERIOD COVERED QUARTERLY REPORT NO. 2 Sept.14,1977-Dec.13,1977 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) George Schreyer		8. CONTRACT OR GRANT NUMBER(s) DAABO7-77-C-0431
9. PERFORMING ORGANIZATION NAME AND ADDRESS TRW Inc., Semiconductor Division 14520 Aviation Blvd. Lawndale, Calif. 90260		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 2779811
11. CONTROLLING OFFICE NAME AND ADDRESS Communications Systems Procurement Branch Procurement and Production Directorate US Army Electronics Command Fort Monmouth, New Jersey 07703		12. REPORT DATE January, 1978 13. NUMBER OF PAGES 16
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Commander DCASMA Los Angeles 9920 South La Cienega Blvd. Inglewood, Calif. 90301		15. SECURITY CLASS. *(of this report)* Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

Approved for public release. Distribution unlimited.

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

DDC
JUN 16 1978
F

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Pin Epi
Vias
Buffered Epi
Monolithic Matching Networks
Spreading Resistance Probe

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Wire bonding experiments on existing microwave dice were performed to determine optimum bonding configurations for microwave transistors. The results of these experiments guided the design of the active portion of the monolithic 2 GHz device, the L-10.

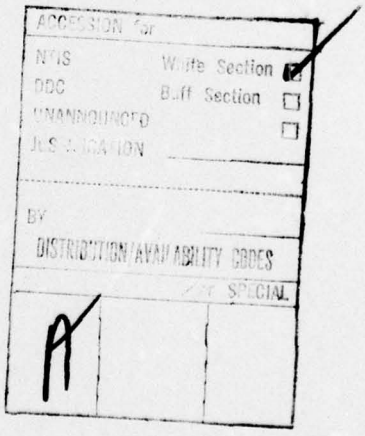
To define a 4 GHz material specification, several lots of 4GHz dice are being processed. The results of experiments on epitaxial resistivity and profile will guide the specification of PIN epitaxial material for the 4GHz portion of the program.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE *(When Data Entered)*

TABLE OF CONTENTS



SECTION I

1.0 PURPOSE

The purpose of this program is to provide for the production of two separate state-of-the-art solid state devices. They are bipolar microwave power transistors with integral monolithic matching networks to be used in amplifier applications. These devices will be configured in such a way as to allow the attachment of the monolithic transistor chip directly to a metal heat sink, thus eliminating the BeO insulator which is typically found in existing microwave power transistor packages.

The two devices to be produced are a 20W/2GHz device and a 5W/4GHz device. These two devices are to operate in the CW mode.

Sufficient quantity of these devices will be fabricated to demonstrate the production feasibility of the basic design and assembly techniques.

SECTION II

TECHNICAL NARRATIVE

2.0 INTRODUCTION

During the second period of the contract, work continued in two areas. The L-10 design was tooled and the first lot started and work continued on SB-4000 processing.

2.1 L-10 MASK SET

The L-10 device, Figure 1, was designed and the drawings were submitted for tooling during the first period of work. The time required for tooling the set was approximately six weeks so that working plates were received halfway through this reporting period. Multilayer epitaxial material had been previously ordered and was received about the same time as the masks. SRP (spreading resistance probe) data, Figure 2, taken on a sample of the silicon material lot indicated that much of the material was unusable due to inadequate resistivity or thickness of the various layers. The spreading resistance profile of a typical sample of unusable material and acceptable material is shown in Figure 2. The vertical scale is spreading resistance in ohms, which is converted to resistivity through a computer program and correlation to resistivity standards. Also, all of the wafers had a substantial edge crown as a residue of the epitaxial process. The edge crown, Figure 3, is a 0.5 to 3.0 mil ridge around the edge of the wafer. A crown will

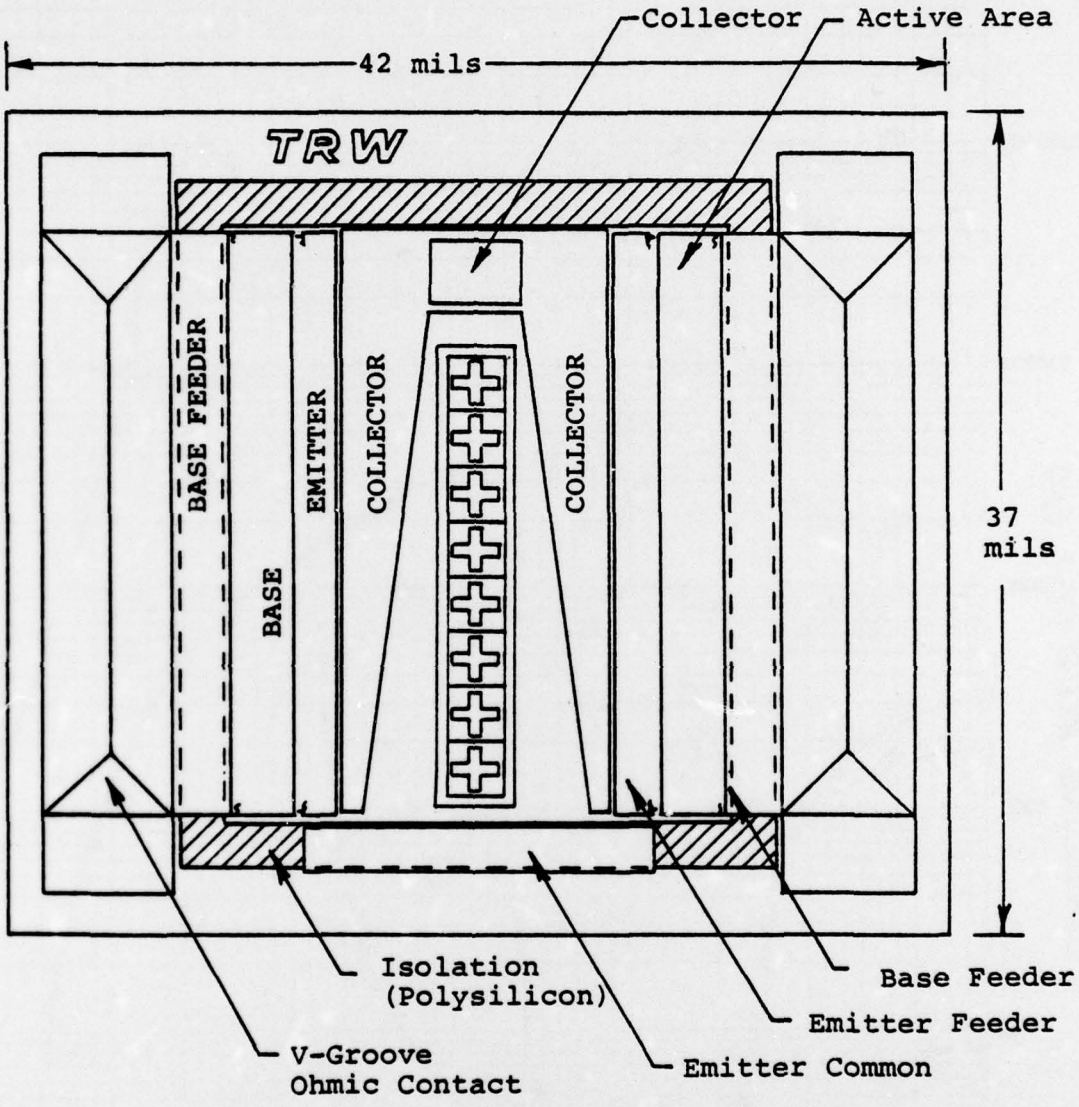


Figure 1. L-10 Device Layout

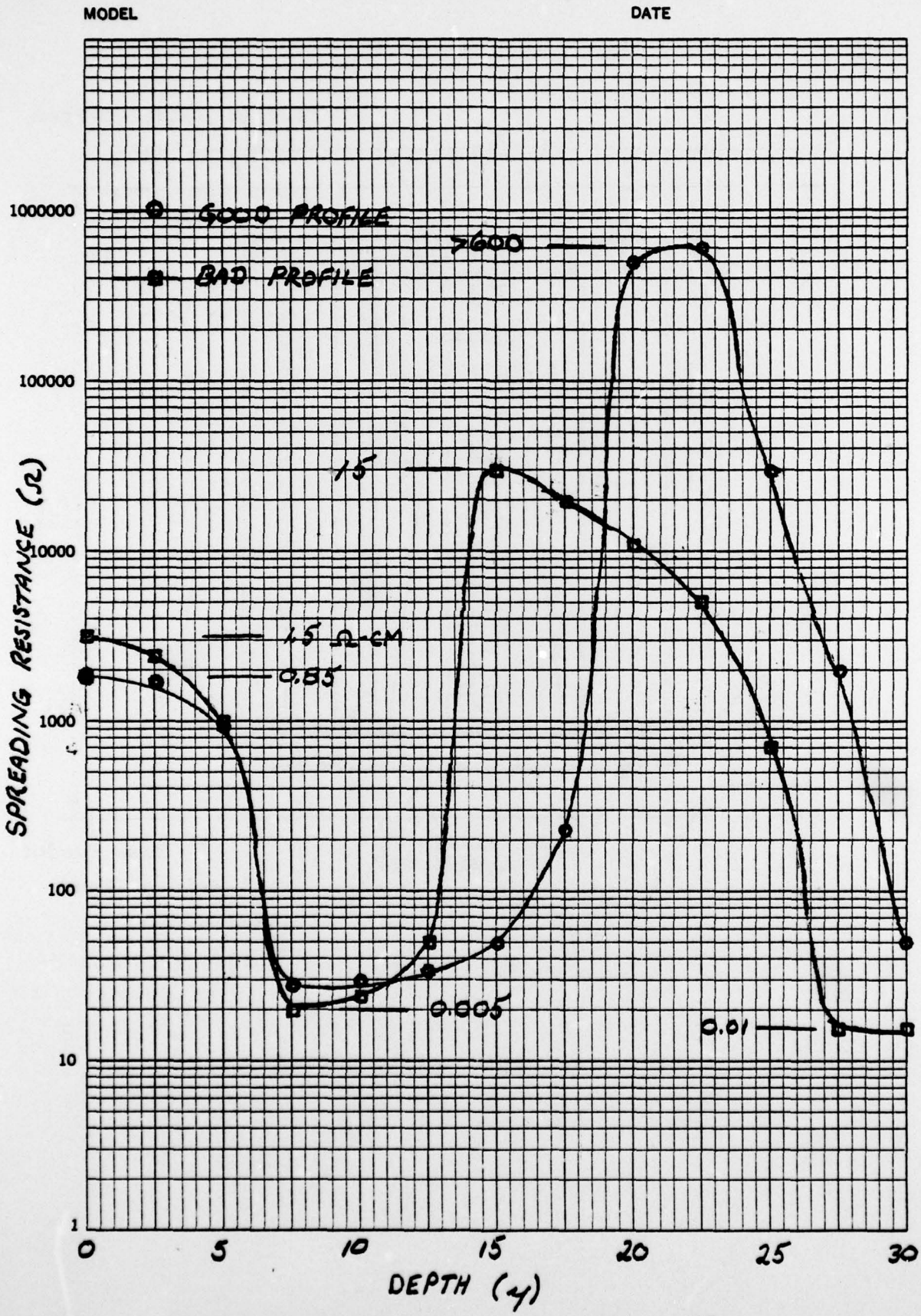


Figure 2. Spreading Resistance Profile

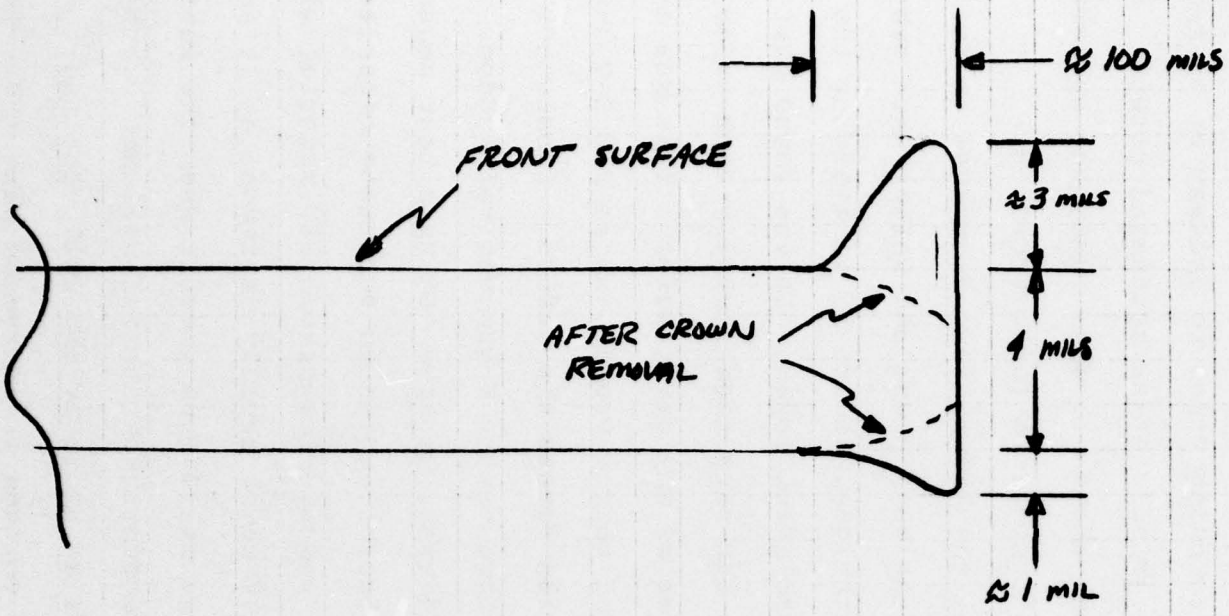


Figure 3. Edge Crown

prevent proper mask contact during subsequent processing. The crown on these wafers was removed by a lapping process which is very time consuming. Deleterious crowning can be prevented in epitaxial growth with proper pre-edge rounding prior to epitaxy or by removal of the crown on a wafer edge grinder after epitaxial growth. Presently, the epitaxy vendor has chosen to edge round the substrate prior to epitaxial growth to compensate for overgrowth.

After crown removal the wafers were V-grooved to form the isolated regions, Figure 4. At this point the wafers were subjected to analysis by a C-V plot technique, Figure 5, to evaluate the characteristics of the PIN isolation layer. It was found that characteristics of the isolation can vary significantly from wafer to wafer and over different areas of any given wafer. This was especially evident with our second source vendor, whose PIN C-V characteristics had extreme variation across the wafers. Subsequent 100% C-V analysis of our prime source vendor V-grooved wafers does not show the wide variations. However, we have set up a test sequence that measures the device collector region to substrate capacitance at 1V and 10V and BV_{cs} @ 100 volts. Acceptable PIN material will have a large capacitance at 0V which rapidly decreases at 1V and becomes independent of voltage at 10V and greater when the intrinsic layer is fully depleted. Unacceptable material will not exhibit a rapid decrease of capacitance at about 1V and will continue to decrease in capacitance as the voltage is increased past 10V. This

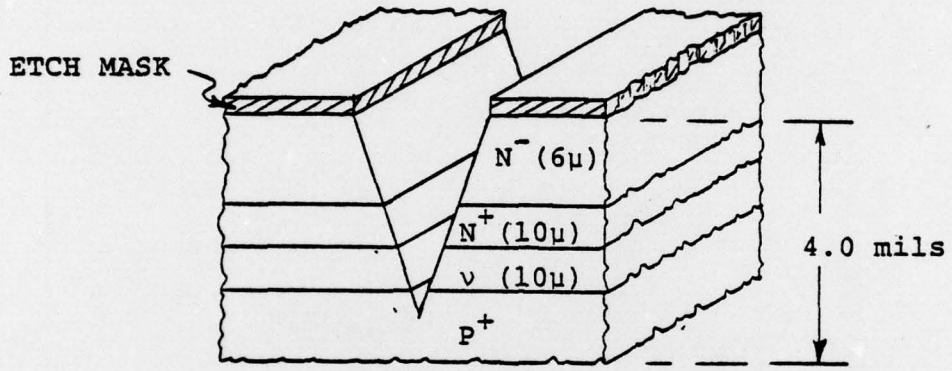


Figure 4. V-Groove Horizontal Isolation

K•Σ 10 X 10 TO ½ INCH • 7½ X 10 INCHES
KEUFFEL & ESSER CO. MADE IN U.S.A.

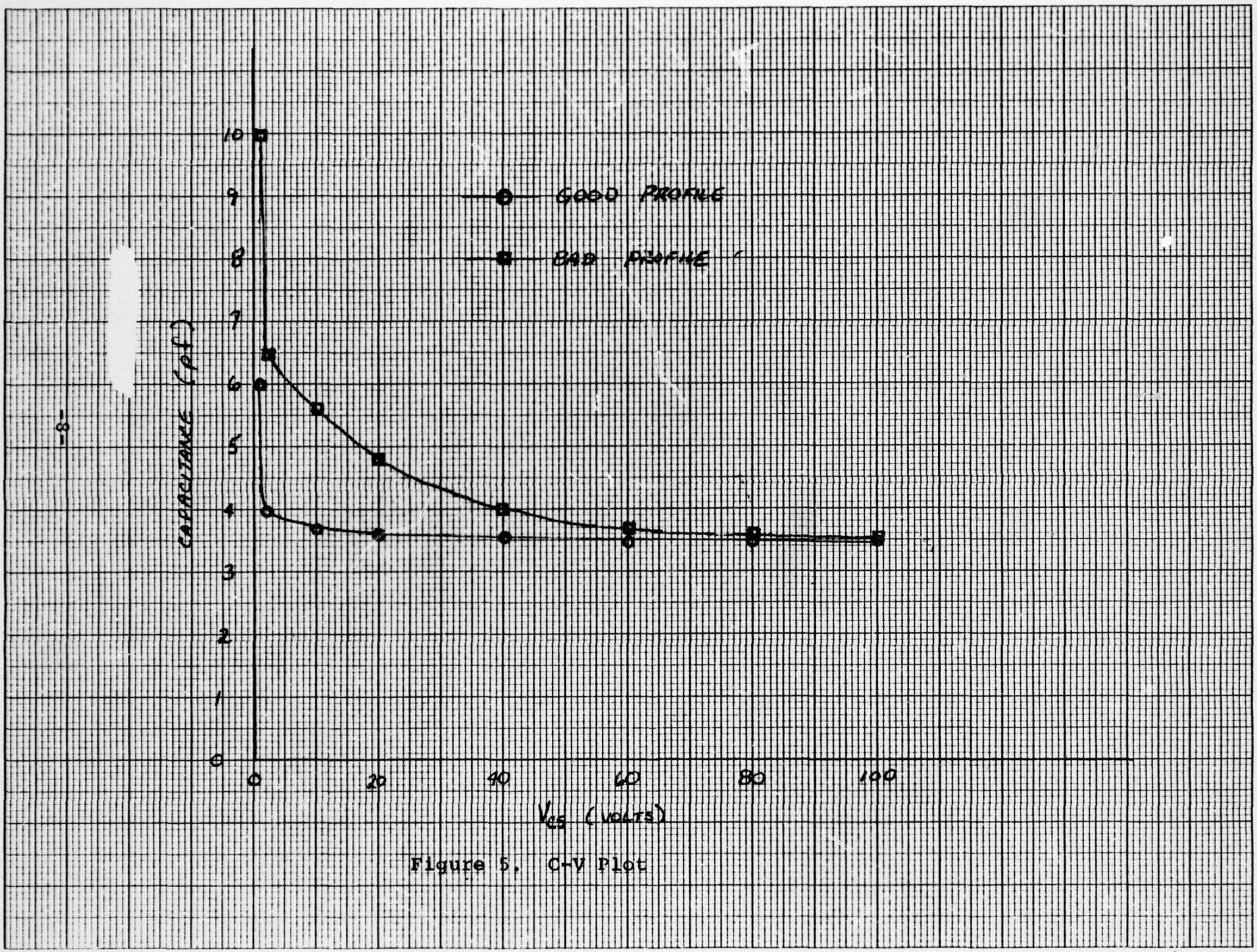


Figure 5. C-V Plot

indicates a graded intrinsic layer profile. The absolute value of the capacitance when fully depleted indicates the thickness of the intrinsic layer.

The first lot of wafers should be ready for test in April, barring any further difficulties.

2.2 L-10 PROCESS DEFINITION

A step by step process outline of the process necessary to produce the L-10 device is shown in Figure 6. This outline shows the process sequence of manufacturing and inspection operations. At each step, a critical process parameter marked with a square or triangle is measured and recorded.

2.3 PROGRESS OF 4GHz MATERIAL SPECIFICATION

Lot BL-5 is the only lot of SB-4000 dice which has reached completion. Lot BL-4 was scrapped at metal and lot CCL-1 was scrapped at emitter. Lots CCL-2, -3, -4 and -5 are still in process. Lot BL-5 was built on epitaxial material which had been back diffused in order to reduce the thickness of the epitaxial layer.

An analysis of the resistivity profile was done using the SRP. This profile, Figure 7, is significant in that the dice from BL-5 produced the same saturated power and efficiency at 5GHz as the best previous devices. We feel that saturated power capability is very dependent on proper epitaxial profile. Since the saturated power of these devices is good, we feel that this profile

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

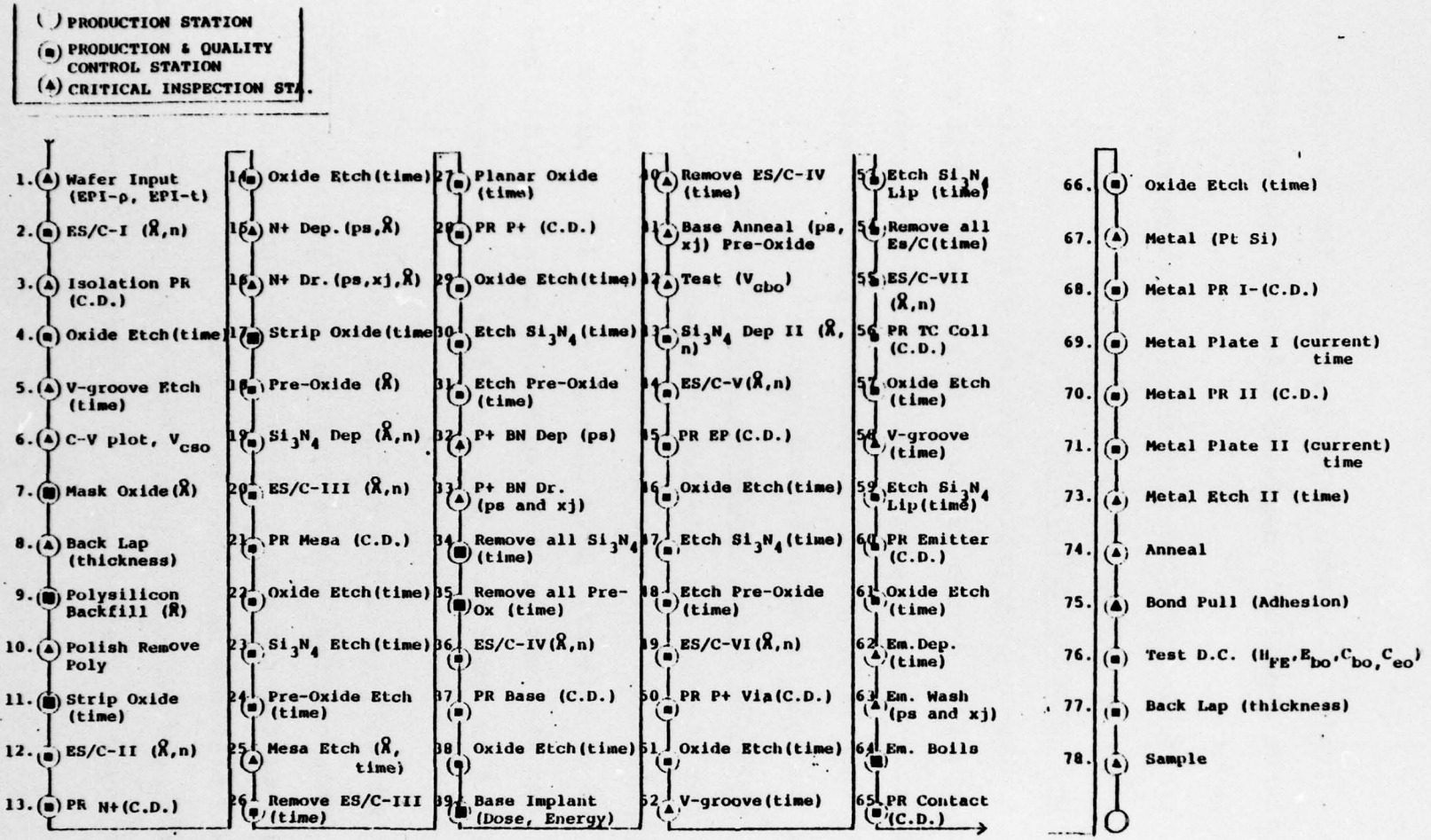


Figure 6. Process Flow Chart L-10 Circuits.

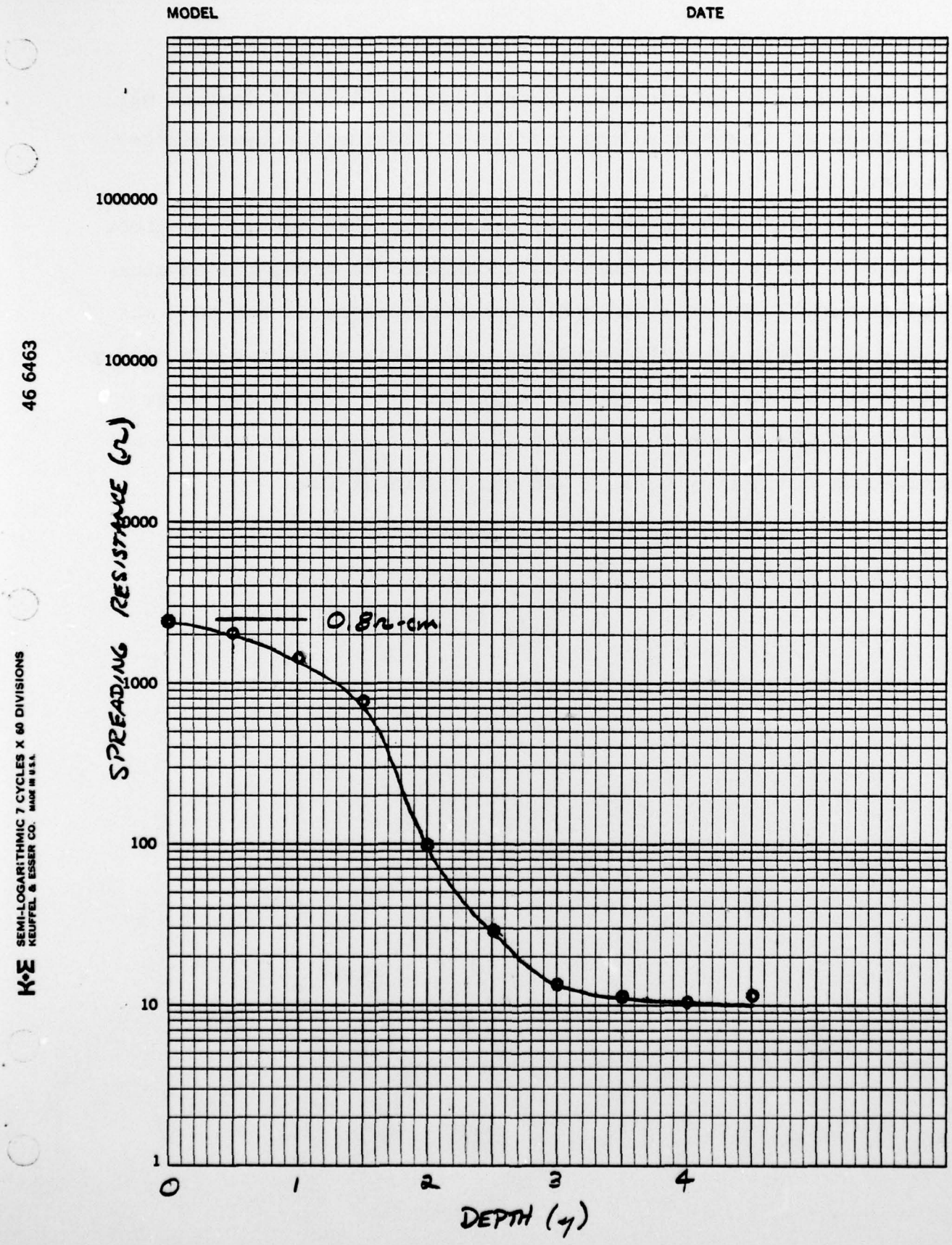


Figure 7. Resistivity Profile

is very close to an optimum. Future lots of SB-4000 devices will be processed to optimize the profile to provide the best performance.

Lot BL-5, however, had lower gain than desired by about 2 to 3dB. This loss in gain was attributed to excessive emitter ballasting, 2.25 times desired. The performance of lot BL-5 was 1.2 - 1.3 watts per cell saturated power at a collector efficiency of 23 to 24% and a gain of 4dB at 5.0GHz. At 4.0GHz the power output of the device increased to 1.6 - 1.7 watts per cell at a collector efficiency of 31 - 32% and a gain of 6dB.

SECTION III

CONCLUSIONS

3.0 L-10 PROCESSING

Processing of the L-10 design is proceeding, although there are problems in the control of the growth of the epitaxial material. Excellent material had been received in the initial R&D work for NRL Contract #N000014-75-C-0405, however, this material was fabricated by our engineers using facilities no longer available to us. Material grown by present vendors without our direct supervision, while not nearly as good, is acceptable to continue work at this point in the program.

3.1 SB-4 PROCESSING

Processing of SB-4000 dice to optimize the collector material specification also continued in order to demonstrate reproducibility. Devices produced thus far have shown excellent collector characteristics.

SECTION IV

PROGRAM FOR THE NEXT INTERVAL

4.0 The effort on the program for the next interval will include the processing of L-10 devices. The first lot is expected in mid-February. Characterization of the first lot will be done to evaluate its performance and obtain impedance data for the network design phase.

Work will be completed on optimization of the collector material for the 4GHz devices, and design of the monolithic chip will be initiated.

SECTION V

PUBLICATIONS, REPORTS, AND CONFERENCES

A Program Review meeting was held on November 17, 1977. Attendees were as follows:

Government

Horst Gerlach, Harry Diamond Labs

TRW

David Wood, R&D Manager
Richard Allison, Program Manager
Bernie Lindgren, Program Manager
George W. Schreyer, Program Engineer

A Program Review meeting was held on December 8, 1977. Attendees were as follows:

Government

Jim Kelly

TRW

Bernie Lindgren, Program Manager

Monthly Report Nos. 4, 5, and 6 were submitted during this quarter.

SECTION VI

IDENTIFICATION OF PERSONNEL

NAME	HOURS
Joseph Courier	60
Alan Harrington	108
C. C. Lee	250
Bernie Lindgren	77
Jim Scheppele	71
George Schreyer	140
George Skelly	83
Frank Bartel	25
Harold Bjornson	72
Ella Matthews	70
Norman Nissen	65
Eugenia Nunez	177
Irene Wood	65
Stephanie Wesche	65
Dorothy May	100
Lois Reed	35
Bob Jenkins	84